

**REMARKS**

At the outset, the Examiner is thanked for the review and consideration of the pending application. The Final Office Action dated October 10, 2007, has been received and its contents carefully reviewed.

Claims 1, 6, 8, 14, 20 and 24 are hereby amended. No claims are hereby canceled and no claims are hereby added. Accordingly, claims 1-30 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

At the outset, Applicants assert that the Examiner's Final Office Action of October 10, 2007 is improper at least for the following reason. The Examiner raised new grounds of rejection by citing new art against claims 1, 3-8, 10-15, 17-25 and 26-30 and again against claims 2, 9, 16 and 26. No claims were amended in the Response filed March 5, 2007 and in the Appeal Brief filed June 4, 2007. Accordingly, the Examiner cited new art against the claims not necessitated by any amendments. However, Applicants have amended the above noted claims (1, 6, 8, 14, 20 and 24) to further advance prosecution on the instant application.

In the Office Action, claims 1, 3-8, 10-15, 17-25 and 26-30 are rejected under 35 U.S.C. §103(a) as allegedly unpatentable over WO 03/058332 A1 (to Lee et al.)(hereinafter "Lee") in view of United States Patent Application 6,256,077 B1 (to Baek)(hereinafter "Baek"). Claims 2, 9, 16 and 26 are rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Lee in view of Baek and further in view of United States Patent 6,461,899 B1 (to Kitakado et al.)(hereinafter "Kitakado").

The rejection of claims 1 and 3-7 is respectfully traversed and reconsideration is requested. Claims 1 and 3-7 are allowable over the cited references in that each of these claims recite a combination of elements including, for example, "... a first gate redundancy line internal to the display formed on the interlayer insulating layer, and connected electrically with just one of the gate electrodes, one of the gate lines, and both gate electrode and gate line through a first gate contact hole and formed of the same material as one of the source and drain electrodes ... a pixel electrode electrically connected with the drain electrode through the drain contact hole formed in the passivation layer." Lee and Baek do not teach or suggest at least these features of the claimed invention.

Applicants maintain that Lee's elements 170 and 175 are not redundancy lines.

Lee shows a gate pad electrode (170) and a data pad electrode (175) formed on the periphery of the display as shown in Lee Figure 3. This is contrary to the claimed invention. Baek is only offered to show “the gate pad can be formed of chrome material (Office Action at page 3).” In any event, gate pad (26) appears to be formed outside of the display area (Figure 1).

Accordingly, claim 1, and claims 3-7 which depend either directly or indirectly upon claim 1, are believed allowable over the cited references.

The rejection of claim 2 is respectfully traversed and reconsideration is requested. Claim 2 depends from claim 1 and thus necessarily contains all of the limitations of claim 1. Accordingly, claim 2 is allowable over the cited references.

The rejection of claims 8 and 10-13 is respectfully traversed and reconsideration is requested. Claims 8 and 10-13 are allowable over the cited references in that each of these claims recite a combination of elements including, for example, “... a pixel electrode electrically connected with the drain electrode through a drain contact hole formed in the passivation layer; and a gate redundancy line internal to the display formed on the passivation layer, and connected electrically with just one of the gate electrodes, the gate lines, and both gate electrode and gate line through a gate contact hole and formed of the same material as the pixel electrode.” Lee and Baek does not teach or suggest at least these features of the claimed invention.

Applicants’ arguments with respect to the rejection of claims 1-7 apply equally to the rejection of claims 8 and 10-13 and will thus not be repeated herein. Accordingly, claim 8 and claims 10-13, which depend either directly or indirectly on claim 8, are allowable over the cited references.

The rejection of claim 9 is respectfully traversed and reconsideration is requested. Claim 9 depends from claim 8 and thus necessarily contains all of the limitations of claim 8. Accordingly, claim 9 is allowable over the cited references.

The rejection of claims 14, 15 and 17-23 is respectfully traversed and reconsideration is requested. Claims 14, 15 and 17-23 are allowable over the cited reference in that each of these claims recite a combination of elements including, for example, “... forming a first gate redundancy line internal to the display on the interlayer insulating layer electrically connected with just one of the gate electrodes, the gate lines, and both the gate electrode and gate line through a first gate contact hole ... forming a drain contact hole in the passivation layer, and forming a pixel electrode connected electrically with the drain electrode through the drain

contact hole.” Lee and Back do not teach or suggest at least these features of the claimed invention.

Applicants’ arguments with respect to the rejection of claims 1-13 apply equally to the rejection of claims 14, 15 and 17-23 and will thus not be repeated herein. Accordingly, claim 14 and claims 15 and 17-23, which depend either directly or indirectly on claim 14, are allowable over the cited references.

The rejection of claims 24-30 is respectfully traversed and reconsideration is requested. Claims 24-30 are allowable over the cited reference in that each of these claims recite a combination of elements including, for example, “... forming a gate contact hole in the passivation layer, and forming a gate redundancy line internal to the display connected electrically with just one of the gate electrodes, the gate lines, and both gate electrode and gate line through the gate contact hole.” Lee, Back and Kitakado do not teach or suggest at least these features of the claimed invention.

Applicants’ arguments with respect to the rejection of claims 1-23 apply equally to the rejection of claims 24-30 and will thus not be repeated herein. Accordingly, claim 24 and claims 25-30, which depend either directly or indirectly on claim 24, are allowable over the cited references. Furthermore, Applicants note that Kitakado is introduced by the Examiner to show, “Kitakado et al. do disclose top gate and bottom gate type structure is known structures for a TFT manufactured on a glass substrate (Office Action at page 3).” As best presently understood, Kitakado does not render the above claims obvious.

Applicants believe the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: October 31, 2007

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